

High-Power Quasi-vertical GaN Schottky Barrier Diode RF Rectifier Based on Impedance Compression Network for WPT Applications

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Abstract— This paper introduces a high-power RF rectifier with excellent adaptability to load variation. The rectifier leverages GaN-integrated quasi-vertical Schottky barrier diodes as the core rectifying components designed for wireless power transfer applications. To address the input impedance fluctuations caused by variations in DC load, the rectifier is integrated into an impedance compression network structure using a quarter-wave impedance transformer. A newly developed diode with a high breakdown voltage of 160 V and an exceptional ideality factor of 1.02 further enhances the rectification performance, particularly at high input power levels. The proposed rectifier achieves a peak power conversion efficiency of 72.6% at 10 W with an efficiency greater than 50% across an input power range from 0.25 to 15.85 W. Additionally, it maintains over 50% efficiency within a DC load dynamic range from 50 to 1100 Ω .

Keywords— RF rectifier, GaN, Schottky barrier diode, high power, quarter-wave impedance transformer.

I. INTRODUCTION

With the rapid development of portable electronics, electric vehicles and implantable medical devices, wireless power transfer (WPT) has attracted considerable interest for its potential to enable efficient and reliable energy transmission across various applications [1], [2]. The rectifier, responsible for converting microwave energy into DC output, is a critical component in microwave WPT systems. Studies on rectifier operation [3], [4] have demonstrated that impedance is influenced by key parameters such as operating frequency, input power, and load conditions.

In a microwave WPT system, two factors can significantly affect the RF-to-DC power conversion efficiency (PCE). First, fluctuations in input power due to the uncertain distance between the receiver and the transmitter [5], and second, variations in DC load, both of which can significantly alter the RF input impedance. This impedance variation poses challenges to achieving effective power transfer and maintaining low reflection [6]. To achieve high PCE, engineers compress the matching impedance variation by employing an impedance-matching circuit. However, achieving stable impedance matching in RF rectifiers is particularly challenging due to the nonlinear characteristics of commonly used rectifying components such as diodes and transistors [7], [8]. The matching performance of the rectifier is

typically optimized for a specific input power level and an associated optimal load resistance. However, when the DC load experiences dynamic variations, commonly observed in applications such as portable electronics or implantable devices, the matching performance and RF-to-DC conversion efficiency of the rectifier degrade significantly.

In this paper, a high-power rectifying circuit based on an impedance compression network is proposed. The design incorporates a $\lambda/4$ microstrip line impedance transformer to minimize RF input impedance fluctuations caused by variations in DC load, thereby improving rectification efficiency and output DC power. To further enhance the power handling capability of the rectifier, a 160 V high breakdown voltage (V_{br}) quasi-vertical GaN Schottky barrier diode (SBD) is developed with an exceptional ideality factor (n) of 1.02. Leveraging this advanced diode, a 10 W high-power 0.875 GHz rectifier is developed with a peak efficiency of 72.6%. Moreover, the rectifier maintains PCE above 50% region is achieved across a wide load resistance range of 50 to 1100 Ω .

II. RF POWER RECTIFIER DESIGN

A. Schottky Barrier Diode Development

Traditional diodes face challenges in the high current and voltage demands required for high-power RF energy conversion. The relatively narrow bandgaps of materials such as GaAs and Si impose inherent material limitations, restricting their efficiency and capability to operate at high power levels. To address these challenges and achieve high-efficiency, high-power rectification, employing SBD with high V_{br} and an exceptional ideality factor n presents a promising solution. Therefore, a GaN SBD with a quasi-vertical configuration has been developed to implement high-power rectification. The fabrication process involves optical lithography to define an etched region after a standard cleaning process, which is then removed by a dry-etched system with a SiO_2 hard mask. Subsequent surface cleaning using $\text{HCl}+\text{H}_2\text{O}$ eliminates native oxide before proceeding with the Schottky and ohmic metal deposition process. This essential procedure achieves an exceptional ideality factor n of 1.02, enhancing forward characteristics and yielding a higher zero-bias current

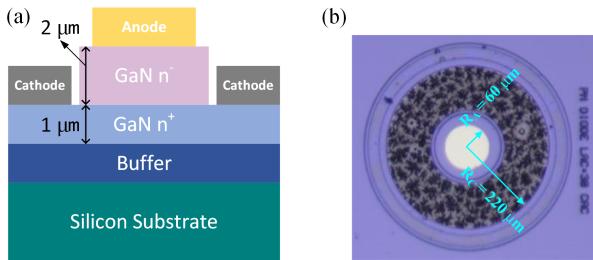


Fig. 1. Proposed high breakdown voltage GaN SBD including (a) Cross-sectional schematic view of the GaN on Si substrate SBD and (b) the fabricated ring diode top view with radius inserted.

responsivity \mathfrak{R}_{I0} . Notably, the PCE is directly proportional to \mathfrak{R}_{I0} [9]. The parameter \mathfrak{R}_{I0} can be expressed as:

$$\mathfrak{R}_{I0} = \frac{q}{2n k_B T} \quad (1)$$

where q is the electron charge, k_B is the Boltzmann constant and T is the operating temperature.

The low 0.7 eV Schottky barrier height of the anode contact plays a crucial role in achieving a low V_{on} , which is beneficial in enhancing efficiency at the low input power range [10]. The combination of both polarities in the GaN surface under the Schottky contact may contribute to a decrease in the extracted Schottky barrier height.

A cross-sectional schematic of the fabricated SBD is depicted in Fig. 1 (a), with a top-view depiction of its dimensions (Fig. 1 (b)). The epitaxial structure consists of an AlGaN buffer layer, a 2 μm n⁻ GaN drift layer and a 1 μm n⁺ layer, all fabricated on a 6-inch Si substrate using metal-organic chemical vapour deposition. This design is cost-effective, as it eliminates the need for free-standing substrates, and also improves device stability compared to lateral AlGaN-on-GaN configurations [11]. The anode contact achieves a low Schottky barrier height of 0.7 eV, contributing to the ultra-low V_{on} . Notably, the GaN surface beneath the Schottky contact consists of both N and Ga polarities, which further reduces the effective barrier height. The short distance between the anode and cathode lowers V_{on} and the series resistance (R_s), facilitating improved lateral electron flow across the drift layer. Fig. 2(a) shows the linear-scale forward current density vs. voltage (J - V) and R_{on} - V characteristics of the SBD. The on-resistance is measured to be $1.75 \pm 0.10 \text{ m}\Omega\cdot\text{cm}^2$, with a R_s of 10Ω . Fig. 2(b) presents the log-scale forward bias J - V characteristics. An n of 1.02 reflects high-quality contact formation, and the average V_{on} is observed at 0.23 V, where J reaches $1 \text{ A}/\text{cm}^2$. The reverse I - V characteristics of the GaN diode are displayed in Fig. 2(c). A high V_{br} of 160 V is achieved, which is highly beneficial for high-power rectification. Compared to the analogous design in the previous study achieving a 45 V breakdown voltage [12], this device attains a significantly higher reverse voltage (160 V), attributed to the thicker 2 μm n⁻ drift layer and lower carrier concentration ($1.0 \times 10^{16} \text{ cm}^{-3}$). Fig. 2(d) illustrates the total capacitance across the SBD. A C_j of 4.5 pF is attained at a bias voltage of 0 V.

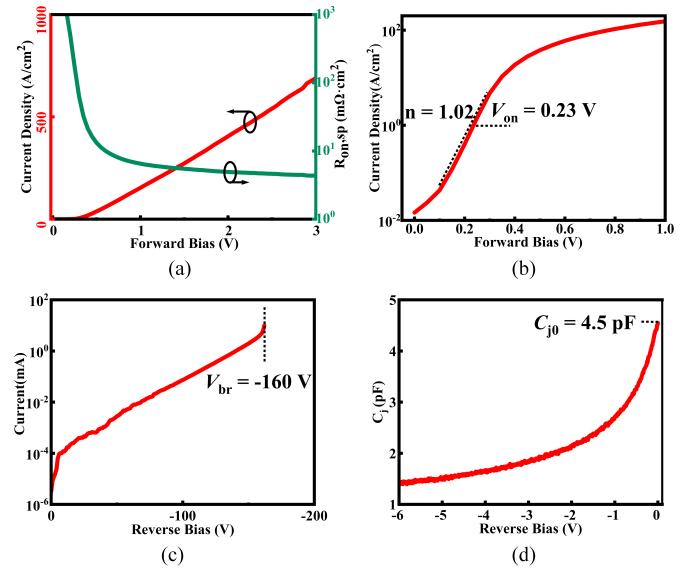


Fig. 2. Typical performance of the quasi-vertical GaN SBD: (a) forward current density (J) vs. forward voltage and the corresponding specific on-resistance of the SBD; (b) logarithmic plot of forward bias $V_{on} = 0.23 \text{ V}$ @ $J = 1\text{A}/\text{cm}^2$ and $n = 1.02$; (c) reverse current vs. reverse voltage; (d) total capacitance vs. reverse voltage.

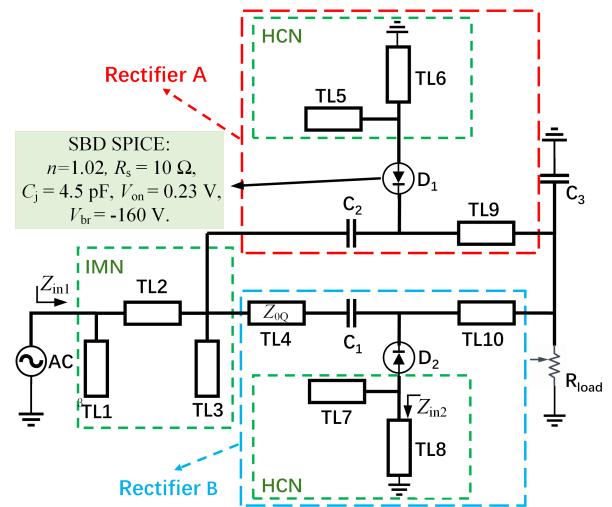


Fig. 3. Topology of the proposed high-power RF rectifier with an impedance transformer network.

B. Rectifier Design

Fig. 3 illustrates the schematic of the proposed impedance compression network based rectifier. This design addresses a critical challenge in WPT systems: the substantial variation in RF input impedance caused by fluctuations in the DC load. Such variations can degrade power transfer efficiency and stability. By adopting the impedance compression network structure, the rectifier effectively mitigates impedance fluctuation, ensuring consistent RF-to-DC conversion efficiency across a wide range of operating conditions. The proposed rectifier system includes a shared impedance-matching network (IMN, TL1-TL3), a $\lambda/4$ impedance inverter (TL4), and harmonic compression

Table 1. Microstrip Transmission Line Electrical Parameters.

	TL1	TL2	TL3	TL4	TL5	TL6	TL7	TL8	TL9	TL10
Z_0 (Ω)	59	93	71	89	50	67	50	70	69	63
Elec. Length (deg)	24	34	18	90	30	45	30	45	90	90

networks (HCNs, TL5-TL8). The design incorporates two DC-blocking capacitors (C_1, C_2), two identical GaN SBD (D_1 and D_2) with two $\lambda/4$ transmission lines (TL9, TL10) ending with C_3 and a DC load R_{load} that form an open circuit at the fundamental frequency. The electrical parameters for each transmission line are provided in Table 1.

In the proposed rectifier design, a standard shunt rectifier (Rectifier A) is connected in parallel with an identical rectifier (Rectifier B), linked via a quarter-wave impedance transformer (TL4). The relationship between the input impedance $Z_{\text{in}1}$ and R_{load} of the impedance compression network rectifier can be expressed as:

$$Z_{\text{in}1} = \begin{cases} \frac{R_{\text{load}}}{\alpha Z_{0Q}} & (0 < R_{\text{load}} \leq \alpha Z_{0Q}) \\ \alpha \frac{Z_{0Q}^2}{R_{\text{load}}} & (R_{\text{load}} > \alpha Z_{0Q}) \end{cases} \quad (2)$$

where Z_{0Q} represents the characteristic impedance of TL4, and α is the proportionality constant, determined by the design structure of the rectifier. For Rectifier A, the RF input impedance is directly proportional to R_{load} , while for Rectifier B, the RF input impedance is inversely proportional to R_{load} . As a result, the input signal flows directly into Rectifier A when R_{load} is relatively low or flows to Rectifier B under higher R_{load} conditions. This mechanism allows the proposed rectifier to automatically select the appropriate circuit with lower RF input impedance, effectively minimizing variations in RF input impedance caused by fluctuations in the DC load. As a result, the rectifier maintains a stable low RF input impedance and suppresses instability due to changes in the DC load.

The HCNs consist of $\lambda/12$ (TL5, TL7) and $\lambda/8$ (TL6, TL8) microstrip lines, which are connected in parallel and shorted to the ground. According to the transmission line theory, the input impedance ($Z_{\text{in}2}$) of the short-circuited transmission line at DC, the fundamental frequency, and the second harmonic can be described as follows:

$$Z_{\text{in}2} = j \tan \left(\frac{\pi}{4} \frac{\omega}{\omega_0} \right) Z_{0E} = \begin{cases} 0, & \omega = 0 \\ j Z_{0E}, & \omega = \omega_0 \\ \infty, & \omega = 2\omega_0 \end{cases} \quad (3)$$

where Z_{0E} represents the characteristic impedance of the $\lambda/8$ microstrip transmission lines. At DC, the HCNs act as short circuits, ensuring a direct current path during rectification.

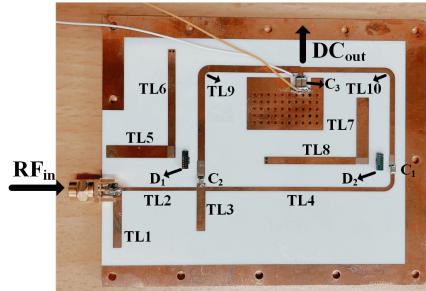


Fig. 4. Photograph of the fabricated high-power RF rectifier prototype.

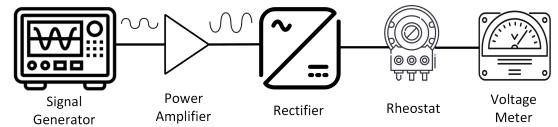


Fig. 5. Configuration diagram of the measurement system.

This characteristic is essential for maintaining the rectification mechanism. The shorted microstrip transmission line exhibits an inductive impedance at the fundamental frequency, this impedance is designed to compensate for the capacitive reactance of the SBD, resulting in a purely real impedance that enhances impedance matching at the fundamental frequency. Simultaneously, TL5 and TL7 contribute to effective impedance matching. At the second-harmonic frequency, TL6 and TL8 function as quarter-wavelength transmission lines, effectively transforming the voltage and current across the SBD to achieve harmonic compression behavior.

III. IMPLEMENTATION AND EXPERIMENTAL RESULTS

To validate the design methodology, the proposed rectifier circuit was fabricated and experimentally tested. In this design, a 1.52 mm thick Rogers 4003C substrate is utilized, characterized by a relative dielectric constant of 3.38 and a loss tangent of 0.0027. Fig. 4 illustrates the fabricated rectifier, with dimensions of 91 mm \times 75 mm. An SMC connector is soldered to the RF input port, while two DC cables are connected with a high-power rheostat to the DC output port. The anode and cathode of the diodes are bonded to the microstrip transmission lines. The rectifier operates at a frequency of 0.875 GHz

Table 2. Comparisons with Previous Works.

Refs. / Year	Freq (GHz)	Device	Peak η @ Pin (Watt)	Pin range (Watt) ($\eta > 50\%$)	Load range (Ω) ($\eta > 50\%$)
[13] / 2024	2.5	HEMT	82% @ 10	0.17 - 10	50 - 300 ($\eta > 60\%$)
[14] / 2022	2.45	FET and SBD	74.4% @ 1	0.04 - 2	60 - 730
[15] / 2020	2.45	GaN SBD	78.5% @ 1.9	0.02 - 1.9	20 - 200 ($\eta > 60\%$)
This work	0.875	GaN SBD	72.6% @ 10	0.25 - 15.85	50 - 1100

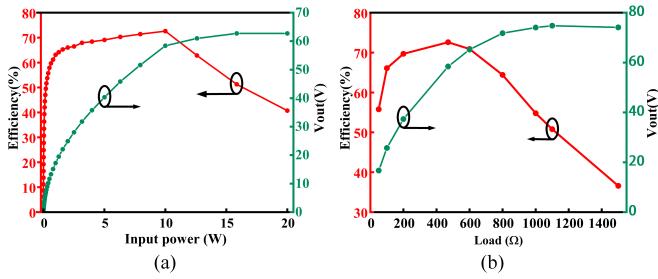


Fig. 6. PCE and V_{out} dependence of the (a) input power and (b) R_{load} .

within the industrial, scientific, and medical (ISM) band. The fabricated rectifier is tested for efficiency and DC output using a testing system (Fig. 5). An RF signal is generated using a microwave source (Rohde & Schwarz SMB100A), amplified through a power amplifier, and delivered to the proposed rectifier. A high-power rheostat (RHS2K5E) serves to absorb the DC power, while a voltage meter (Agilent Keysight 34411A) is utilized to measure the resulting DC voltage with precision.

The rectifier utilizes GaN SBDs with a superior n and high V_{br} for rectification. The main SPICE parameters are provided in Fig. 1 in the previous section. C_1 and C_2 (1 pF) serve as DC blocks, while C_3 is 100 pF. The PCE and the output voltage versus the input power at 0.875 GHz with a load resistance of 470 Ω are depicted in Fig. 6(a). A peak conversion efficiency of 72.6% is achieved at an input power of 10 W. Meanwhile, the rectifier circuit achieves a PCE of 51.2% at an input power of 15.85 W, highlighting a significant improvement in high-power handling capacity compared to conventional Si and GaAs diodes, which achieve the same 50% efficiency at much lower input power levels. Fig. 6(b) depicts the dependence of PCE and V_{out} on R_{load} at an input power of 10 W. As expected, a $PCE > 50\%$ is observed within a R_{load} range from 50 to 1100 Ω . Table 2 shows the comparison of the maximum efficiency with input power, input and load dynamic range between the proposed high-power rectifier and previous works [13]–[15]. Thanks to the innovative impedance compression network structural design and the unique characteristics of GaN SBDs, the proposed rectifier demonstrates exceptional performance, featuring high power-handling capability and strong adaptability to varying DC loads.

IV. CONSLUSION

This paper presents the development of a high-power RF rectifier utilizing a GaN Schottky barrier diode with a superior ideality factor of 1.02 and a high breakdown voltage of 160 V, specifically designed for far-field wireless power transfer applications. The impedance compression network design effectively mitigates the effects of DC load variations and minimizes fluctuations in RF input impedance, resulting in significant improvements in RF-to-DC power conversion efficiency in wide dynamic range.

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