Rectenna-Enabled New Paradigm With Hybrid Harmonic Beamforming for Integrated Energy Harvesting, Sensing, and Communications

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***Abstract*— Given the swift advancement of the Internet of Things (IoT) and wireless power transfer (WPT), there is an increasing need for incorporating new functionalities such as wireless communication, recognition, sensing, and localization into existing systems. In response to these evolving demands, a transformative rectenna-based unified platform has been developed. This groundbreaking platform is engineered to harvest ambient wireless power while smartly managing the generated second-order harmonic signals. Illustrating its design, a multi-functional system has been implemented. This system can convert 52.9% of input radio frequency (RF) power into direct current power and achieve a state-of-the-art SH generation efficiency of 10.2% when the input RF power is set at 0 dBm. Concurrently, the harmonic signals can be re-radiated and automatically directed (steered) from −65° to 66°, facilitated by an 8 × 8 Butler matrix and an 8-way microwave switch, all controlled by a microcontroller unit (MCU). Notably, our platform extends beyond beamforming to embrace a broader spectrum of applications, including backscattering communication, simultaneous wireless information and power transfer (SWIPT), integrated sensing and communications (ISACs), and continuous wave detection. This expansion significantly enhances the scope and capability of rectification technology applications.**

***Index Terms*— Harmonic beam steering, radio frequency (RF) energy harvesting, rectifier, second-order harmonic generation (SHG).**

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I. Introduction

INTERNET of Things (IoTs) as a medium of information exchange, can contact the functional terminals including discrete wireless sensors and controllers through a network [1], [2], [3]. To improve their synergy efficiency, timely sharing of the identified information is necessary as well as maintaining long-term uptime, often resulting in the separation of the communication system and the power supply module [4], [5], [6], [7]. This system layout places a barrier to enhance the system integration, and the extra electric devices always lead to a drop in standby time of the various nodes [8], [9]. Therefore, merging these two modules to simultaneously supply power and generate carrier signals could significantly mitigate this issue. Such an integration would not only address the current limitations but also foster further development in IoT applications, as suggested in [10].

The proliferation of ambient wireless signals, including 5, 4 G, and Wi-Fi, as indicated in references [11], [12], [13], [14], [15], highlights an opportunity. A nonlinear rectifier can convert radio frequency (RF) power into direct current (dc) energy and harmonics simultaneously. This approach presents a promising solution to the problem previously mentioned, as discussed in references [16], [17], [18], [19], [20]. Building on this strategy, various efforts have been undertaken to design duplex rectifiers capable of generating both dc power and carrier signals concurrently. For example, a charge pump was presented in [21], integrating two identical voltage doublers and a modified rat-race coupler, by which 71.3% RF-dc power conversion efficiency was achieved while the second-harmonic generation (SHG) efficiency only reached 0.04% even at a high input power level of 19 dBm. In the following, in [22] and [23], two compact duplexing rectennas were proposed to improve the SHG efficiency. However, the efficiency of SHG achieved was limited due to the absence of an optimized output matching network for transmitting the generated harmonics. Specifically, the realized SHG efficiency was recorded at only 1.26% at 5 dBm as per [22], and 2.51% at 15 dBm according to [23]. Recently, a new architecture of a single-port harmonic transponder with a stub-based duplexing structure was proposed in [24], in which to further improve the SHG, a quarter-wave and a one-eighth-wave transmission line were

adopted to isolate the fundamental RF (FRF) and the SH signals, avoiding the SH being second rectified. Based on the well-designed rectifier, the SHG efficiency was up to 6.3% as the input power was 0 dBm. In addition, a duplex rectifier with excellent SHG efficiency (10.4%) was achieved with the help of the source pull technology [25], while considering its FRF input and SH output share a common port, it is still faced with the challenge to manipulate the generated harmonics flexibly. From the above discussion, it is evident that with the efforts of the peer researchers, the SHG efficiency of the duplex rectifier has been significantly improved, but regarding a real Schottky diode it was realized that the SHG limit was still lacking research. That is to say, it is difficulty to tailor the optimized design without a visible target. In addition, the existing harmonic-based application is also restricted by the simple system, and therefore, to drive it from lab to fab, more complex applications also should be implemented considering the real requirements.

In this article, to solve the aforementioned problems, a multifunctional rectenna system was proposed, designed to efficiently generate both second-order harmonic (SH) and dc power, as well as to automatically control the beam behavior of the SH. To guide the design of the duplex rectifier, the theoretical limits and influencing factors of harmonic generation (HG) efficiency for commonly used rectifying diodes were thoroughly investigated. Leveraging this knowledge, load pull and source impedance pull techniques were employed in the design process of the duplex rectifier. This meticulous approach resulted in a duplex rectifier that achieves an RF-dc conversion efficiency of 55.2% and a groundbreaking SHG efficiency of 10.47% at an input power level of 3 dBm at a 2.6-GHz frequency for the RF input. Then for implementing the classical beam control functionality—beam steering, a common aperture dual-band antenna array for receiving the FRF energy and radiating the generated SH signal, and an 8 × 8 Butler matrix was designed and connected together with the predesigned duplex rectifier. Finally, with the help of the total system, the generated SH beam to the best of our knowledge was first tuned in a large angular span—65° to 66°, reflecting the great potential in practical applications. Compared to the common harmonic transmitting rectennas that only send the generated signals, our design can manage or control the SHG signal at the Rx side flexibly, enabling brand new applications in both node tracking and backscatter communications.

II. Duplex Rectifier Design

A. HG Efficiency Analysis

In [26], the limiting HG efficiency of a Schottky diode has been theoretically proved as $1/m^2$ (where m denotes the harmonic order) by analogically analyzing an ideal nonlinear resistance, while regarding a real Schottky diode, its HG efficiency limitation is still lacking research. Therefore, before constructing the proposed multifunctional rectenna system, we first uncovered the effect of the diode series resistance (R_s) on the HG efficiency through a classical shunt diode topology consisting of a diode (SMS7630 with R_s and forward voltage (V_F) of 20 Ω and 0.18 V at 1 mA, respectively) [27], a dc feed, a dc block, and a RF source, as shown in Fig. 1(a). It is important to note that since our system was specifically designed to generate and control the SH, the subsequent analysis primarily focused on the efficiency of SHG. This aspect of the system's performance has been theoretically proven to achieve a value of 25%. In this setup, the dc block functions as an ideal capacitor, serving to prevent the flow of dc energy back to the RF source. Conversely, the dc feed, essentially an ideal inductor, is configured to allow only dc energy to pass through. This design ensures efficient separation and handling of different energy forms within the system. With the help of the dc feed and block, the flow behaviors of the generated dc (orange arrow line) and SH (blue arrow line) at 5.2 GHz, and the FRF (green arrow line) at 2.6 GHz can be confined to the predefined paths [see Fig. 1(a)]. Then, by optimizing the source impedance of RF source ($Z_1 = R_1 + jY_1$), the generated SH can be completely guided out from Port 1 along the blue path without losses. During this process, the FRF power into the diode was maintained to a fixed level. To calculate the SHG efficiency, two power probes (P and P′) for detecting the FRF and SH power were added before the diode [see Fig. 1(a)]. The SHG efficiency of the diode was defined as the ratio of the FRF power into the diode to the generated SH power that flows out of the diode, and thereby can be calculated by using the following equation:

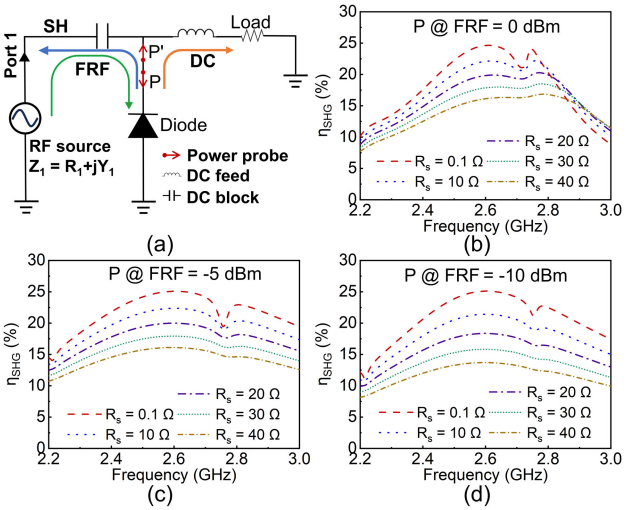

Fig. 1. (a) Classical shunt diode topology for analyzing HG efficiency. SHG efficiency of a diode with different parasitic series resistances as the input power is (b) 0 dBm, (c) −5 dBm, and (d) −10 dBm.

$$SHG\ efficiency = \frac{Output\ SH\ power}{Input\ FRF\ power} \tag{1}$$

where the output SH power can be detected by the power probe P′, and Input FRF power is monitored by the power probe P. Note that the direction of the arrow denotes that only the power flows along this direction can be detected by the corresponding of the power probes shown in Fig. 1(a) conforming to the requirements of (1).

As shown in Fig. 1(b), when P at FRF remains 0 dBm, the SHG efficiency gradually enhances to near the theoretical maximum (24.9% at R_s of 0.1 Ω)—25%, with the decrease of R_s (from 40 to 0.1 Ω). Similar phenomena can be observed regarding different P at FRF [−5 dBm at Fig. 1(c) and −10 dBm at Fig. 1(d)]. Then to demonstrate the generalizabil-

TABLE I
SHG EFFICIENCY FOR DIFFERENT DIODES

Diode	SMS7630 / SMS7621 / HSMS2850		
R_s \ P_{in}	0 dBm	–5 dBm	–10 dBm
0.1 Ω	24.9%/23.5%/-	25%/23.4%/-	24.9%/23.4%/-
10 Ω	22.3%/21.6%/24.3%	22.3%/21.6%/24.1%	21.4%/20.8%/23.6%
20 Ω	20.1%/19.8%/20.8%	19.9%/19.6%/20.8%	18.3%/18.1%/19.5%
30 Ω	17.9%/18.8%/18.5%	17.9%/18%/18.2%	15.8%/16.4%/17.7%
40 Ω	16.4%/17.7%/16.7%	16.1%/16.3%/15.9%	13.7%/14.2%/15.1%

ity of the above conclusion, the R_s-dependent SHG efficiency of other commercial diodes (SMS7621 with R_s and V_F of 12 Ω and 0.29 V at 1 mA; HSMS2850 with R_s and V_F of 25 Ω and 0.25 V at 1 mA), widely used for rectifying [28], [29], also have been calculated through the similar simulation strategy and provided in Table I, from which the similar change law can be observed. Therefore, the above-drawn conclusion can be regarded as a benchmark for diode selection, for example, if more harmonics are needed, a diode with lower R_s needs to be adopted. Based on this conclusion and considering the requirements for high-efficiency rectification and SHG, SMS7630 was finally determined in our system due to its small R_s and relatively low V_F benefit for low-power RF energy harvesting.

B. Duplex Rectifier Design

Then, surrounding the selected diode, a duplex rectifier was designed in this section to simultaneously realize high RF-dc conversion efficiency and SHG efficiency. As shown in Fig. 2(a), a theoretical topology model of the duplex rectifier was first proposed referring to that in Fig. 1(a), in which several ideal components including band-stop filters (BSFs), dc feed, and dc block were introduced to constraint the flow paths of the generated dc and SH at 5.2 GHz, and FRF at 2.6 GHz, favoring for their behavior control. Regarding these two ideal BSFs, one located before Port 2 can only prevent the FRF power from passing through, the other behind Port 1 was just used for isolating the SH. The dc feed and block own the same functionalities to those in Fig. 1(a). Utilizing these ideal components, the input FRF, along with the generated dc and SH, are confined to their respective paths, as indicated by the green, orange, and blue arrow lines. Beyond these ideal components, a strip line and a radial stub [depicted as green parts in Fig. 2(a)] are strategically positioned at the front and back ends of the diode. These elements play crucial roles: the strip line modulates the Q-factor of the rectifier, enhancing its performance, while the radial stub is employed to prevent RF energy from leaking into the ground plane. To optimize the circuit for a low Q-factor, which is advantageous for conducting impedance transformation, detailed attention was given to the length (L1) of the strip line. This investigation is pivotal in ensuring that the rectifier operates efficiently and meets the desired performance criteria in terms of energy conversion and SH signal control.

Considering the Q-factor can be calculated by using the following equation:

$$Q = \left| \frac{Imag(Z_{\text{in}})}{Real(Z_{\text{in}})} \right| \tag{2}$$

where $\text{Imag}(Z_{\text{in}})$ and $\text{Real}(Z_{\text{in}})$ denote the imaginary and real parts of the rectifier's input impedance, Z_{in} was first extracted from the simulated S-parameters, and presented in Fig. 2(b). Then by substituting the simulated Z_{in} that is as a function of L1 into (2), the Q-factor can be obtained. As shown in Fig. 2(c), the simulated Q-factor of the total circuit varies like a cosine function when L1 increases from 0 to 60 mm, which can be attributed to the periodic variation of $\text{Imag}(Z_{\text{in}})$ and $\text{Real}(Z_{\text{in}})$. In this process, the input power of Port 1 was fixed to 0 dBm, and the source impedance was always conjugate to the input impedance of the circuit, which can be proved by the stable 1.0-mW RF power at 2.6 GHz detected by the power probe P_4 [see Fig. 2(c)]. Simultaneously considering the compact size and low Q-factor, 15 mm was chosen as the value of L1. In addition, the proposed circuit was analyzed from the aspect of the load. It can be seen from Fig. 2(d) that as the load resistance increases, the RF-dc and SHG efficiency first increase and then decrease, and they can almost synchronize to reach the maximum value (58.6% at RF-dc, 18.3% at SHG) when the load resistance was equal to 1400 Ω. It is worthy to note that the realized SHG efficiency is very close to that in Table I (20.1% at R_s of 20 Ω), reflecting the correctness of our design strategy [see Fig. 2(a)]. Their little discrepancy can be attributed to the loss of the microstrip structures. The frequency-dependent RF-dc conversion and SHG efficiency of the optimized circuit were also carried out and illustrated in Fig. 2(e). The great RF-dc conversion and SHG efficiency further prove the advancement of our design.

In the following, to implement the total system, a dc-pass filter, an input matching network for guiding the input FRF, and an output matching network serving for transmitting the generated SH will be designed to replace the ideal components in Fig. 2(a).

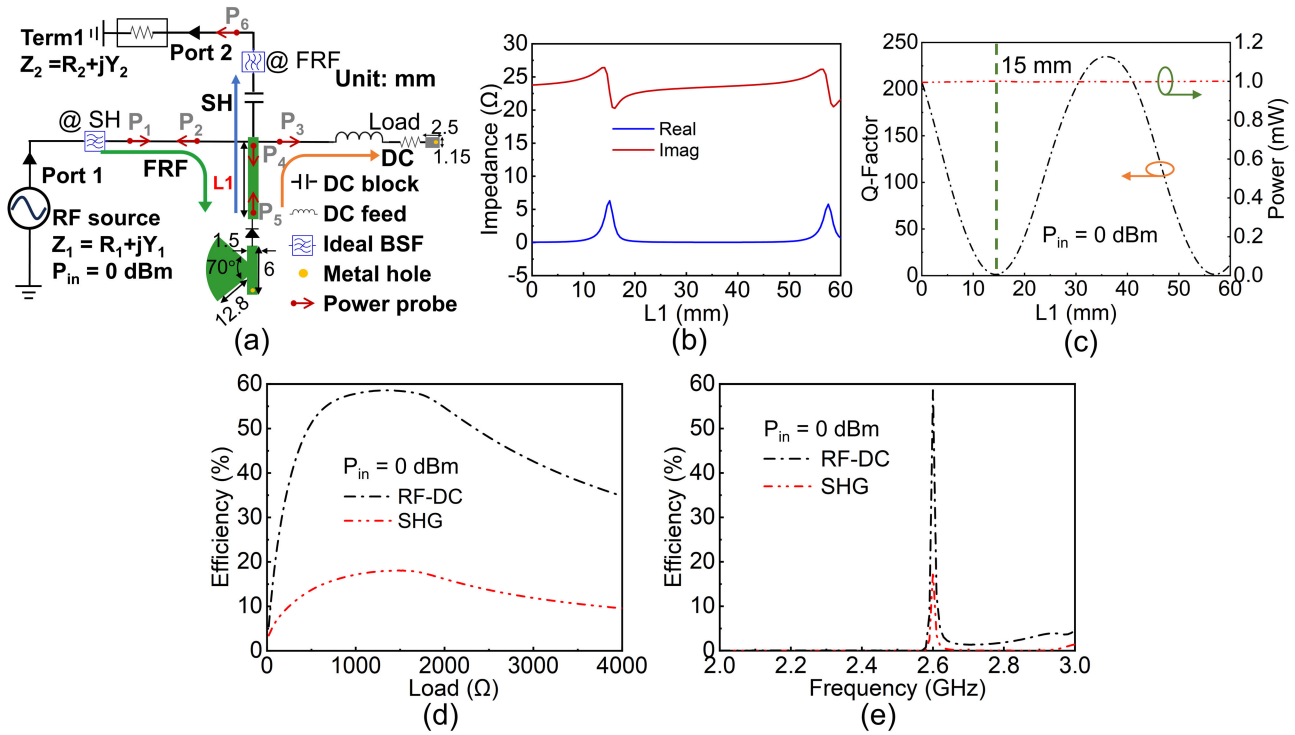

Fig. 2. (a) Proposed topology of the duplex rectifier. Simulated (b) input impedance of the rectifier, (c) Q-factor and power detected by P_4 versus L1. Simulated (d) RF-dc efficiency and SHG efficiency versus load and (e) frequency.

1) DC-Pass Filter Design: To block the FRF and the obtained SH, and pilotage the dc power, a dc-pass filter comprised a strip line [TL0 in Fig. 3(a)] and a radial stub [STUB0 in Fig. 3(a)] was designed to replace the ideal dc-feed [shown in Fig. 2(a)]. In the design process, three power probes (P_1, P_3, and P_5) were added into the circuit shown in Fig. 2(a) for helping calculate the leakage ratio of the input FRF signal and the obtained SH to the load as P_3 at FRF/P_1 at FRF and P_3 at SH/P_5 at SH, respectively. Due to the dimension of the radial stub is related to its operating frequency, as the radius (L2) of the radial stub increases from 0 to 10 mm, the leakage ratio of the FRF [red dotted line in Fig. 3(b)] and SH [black dotted line in Fig. 3(b)] gradually decrease to nearly 0. In the meantime, considering the flow path of the FRF [green arrow line in Fig. 2(a)], when L2 was no less than 10 mm, almost all the input FRF will flow into the rectifying branch [green part in Fig. 3(a)] through observing the ultrahigh ratio calculated as P_4 at FRF /P_1 at FRF [green dotted line in Fig. 3(b)]. Therefore, to efficiently achieve the functionality of the ideal dc feed by the proposed dc-pass filter, 10 mm was selected as the optimum value of L2.

2) Output Matching Network Design: Different from the above dc-pass filter design, for designing an output matching network, in addition to replacing the two ideal components including a dc block and a BSF for isolating the FRF, an impedance transformation circuit is also needed to lead out the generated SH for the following beam control.

To achieve the abovementioned targets, a BSF circuit [blue part in Fig. 4(a)] was first designed to replace the ideal one placed before Port 2 [see Fig. 2(a)], which was used for preventing the FRF from leaking to the ground. The proposed BSF circuit was constructed by TL1 and STUB1 shown in

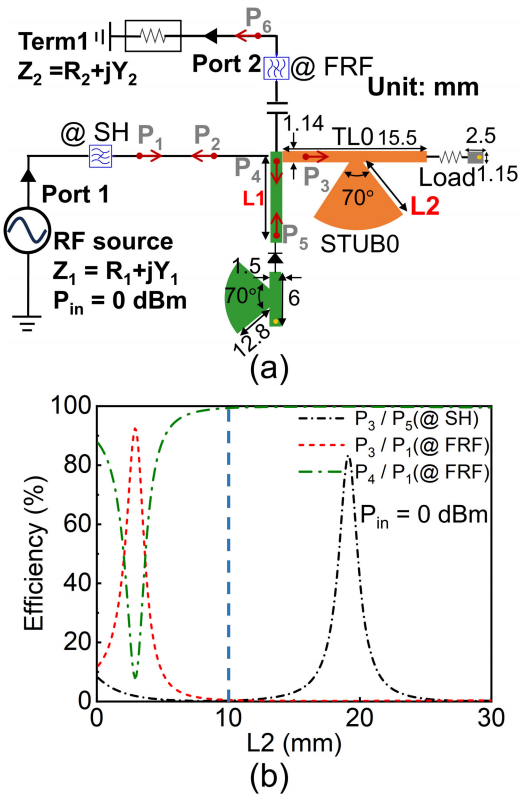

Fig. 3. (a) Construct of the proposed dc-pass filter. (b) Simulated leakage ratio of the FRF input signal and the obtained SH to the load, and the input ratio of the FRF input signal to rectifying branch as a function of L2.

Fig. 4(a). Before evaluating its FRF isolation performance, a term (Term 1) was connected to Port 2, serving as the load impedance of the proposed BSF circuit, and a power probe

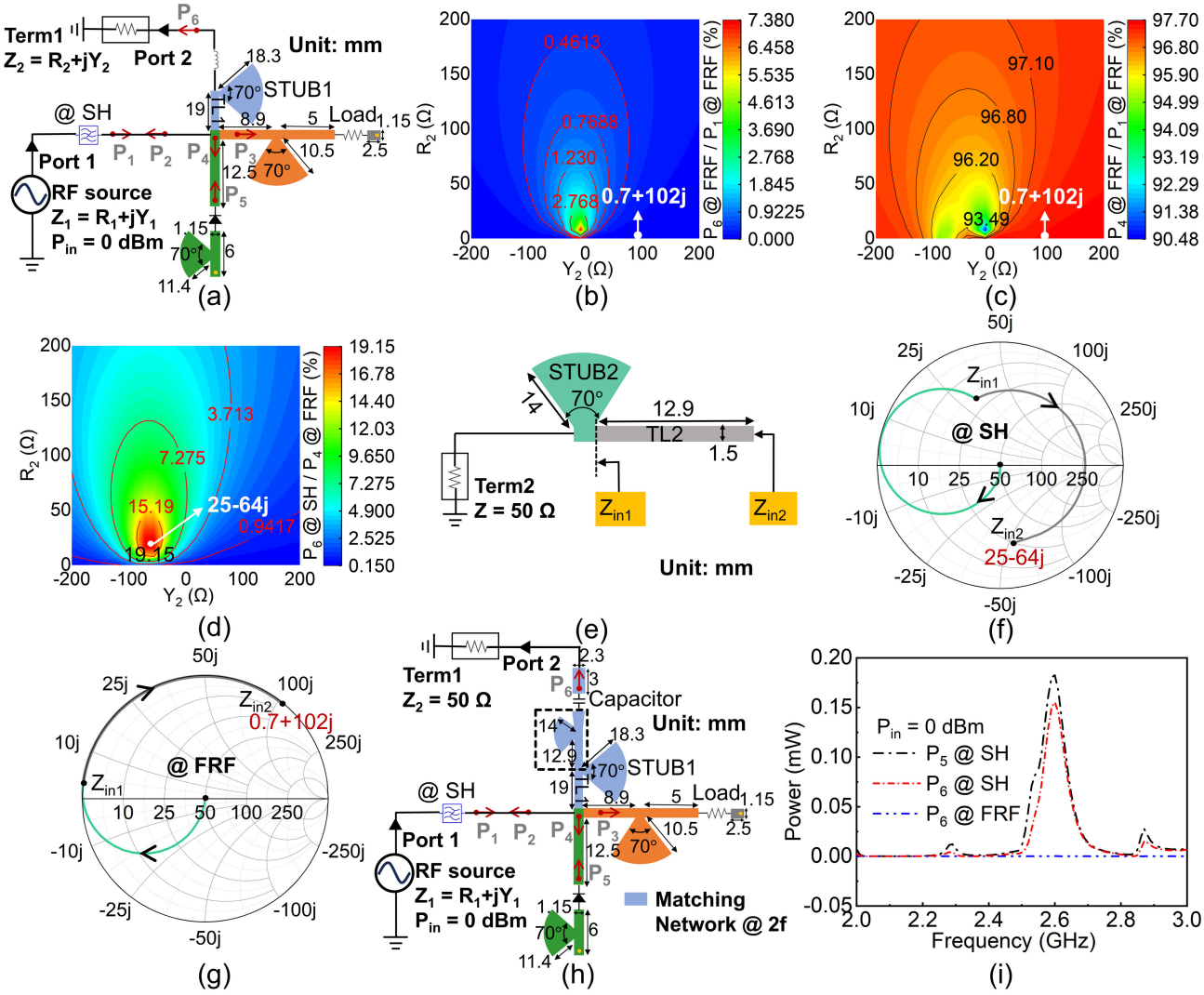

Fig. 4. (a) Design of BSF for 2.6 GHz. (b) Proportion of FRF input signal flowing to the Port 2. (c) Proportion of the FRF input signal flowing to the diode. (d) SHG efficiency versus R_2 and Y_2. (e) Design of impedance transformation circuit. Trajectory changes of Z_{in1} and Z_{in2} on the Smith chart for (f) SH and (g) FRF. (h) Structure of the proposed output matching network. (i) FRF and SH power detected by P_5 and P_6.

(P_6) was located before Term 1 to monitor the leaked FRF. As shown in Fig. 4(b), regardless of the impedance variation of Term 1 ($R_2 + jY_2$), the maximum energy leakage ratio (P_6 at FRF/P_1 at FRF) of the total system is only 7.38% [see Fig. 4(b)], and more than 90.48% (P_4 at FRF/P_1 at FRF) can reach the diode [see Fig. 4(c)], revealing the good performance of the proposed BSF circuit in blocking the FRF.

Next, an impedance transformation circuit [see Fig. 4(e)] will be designed and placed at the back of the BSF circuit [black dotted line frame in Fig. 4(h)] to guide the generated SH. Note that regarding the SH, its input impedance at Port 2 cannot be directly obtained due to the nonreciprocity of the proposed rectifying network [green part in Fig. 4(a)]. Hence, the load pull technique was used to search the optimum output impedance of the SH at Port 2 by varying the impedance of Term 1 shown in Fig. 4(a). It can be seen from Fig. 4(d) that the SHG efficiency calculated as P_6 at SH/P_4 at FRF can reach 19.15% as the output impedance is $25 - 64j\ \Omega$. Due to partial FRF being shunted from Port 2, the calculated SHG efficiency here is slightly higher than that in Fig. 2(d) and (e). Therefore, looking out of the circuit from Port 2 [see Fig. 4(e)], the impedance transformation circuit should transfer the standard $50\ \Omega$ to target impedance ($25 - 64j\ \Omega$) for the SH. To realize this functionality, a radial stub (STUB2) and a transmission line (TL2) were integrated together [see Fig. 4(e)], and their corresponding output impedance transformation process is provided in Fig. 4(f) and (g), in which the input impedance (Z_{in2}) for the SH can be gradually tuned to the optimum value ($25 - 64j\ \Omega$) from $50\ \Omega$ [see Fig. 4(f)]. In addition, with the help of the impedance transformation structure [see Fig. 4(e)], the load impedance of the predesigned BSF circuit for the FRF was transferred to $0.7 + 102j\ \Omega$ [see Fig. 4(g)], which can further improve the FRF isolation performance of this branch referring to the white points in Fig. 4(b) and (c). Subsequently, as the last component of the output matching network, a dc isolation capacitor (10 pF) as shown in Fig. 4(h) was placed at the back of the impedance transformation circuit located inside of the black dotted frame in Fig. 4(h) to replace the ideal dc block. Finally, to evaluate the insert losses of the designed output matching network, the above realized components were merged together [see Fig. 4(h)] and used to replace the originally ideal topology [see Fig. 3(a)]. From

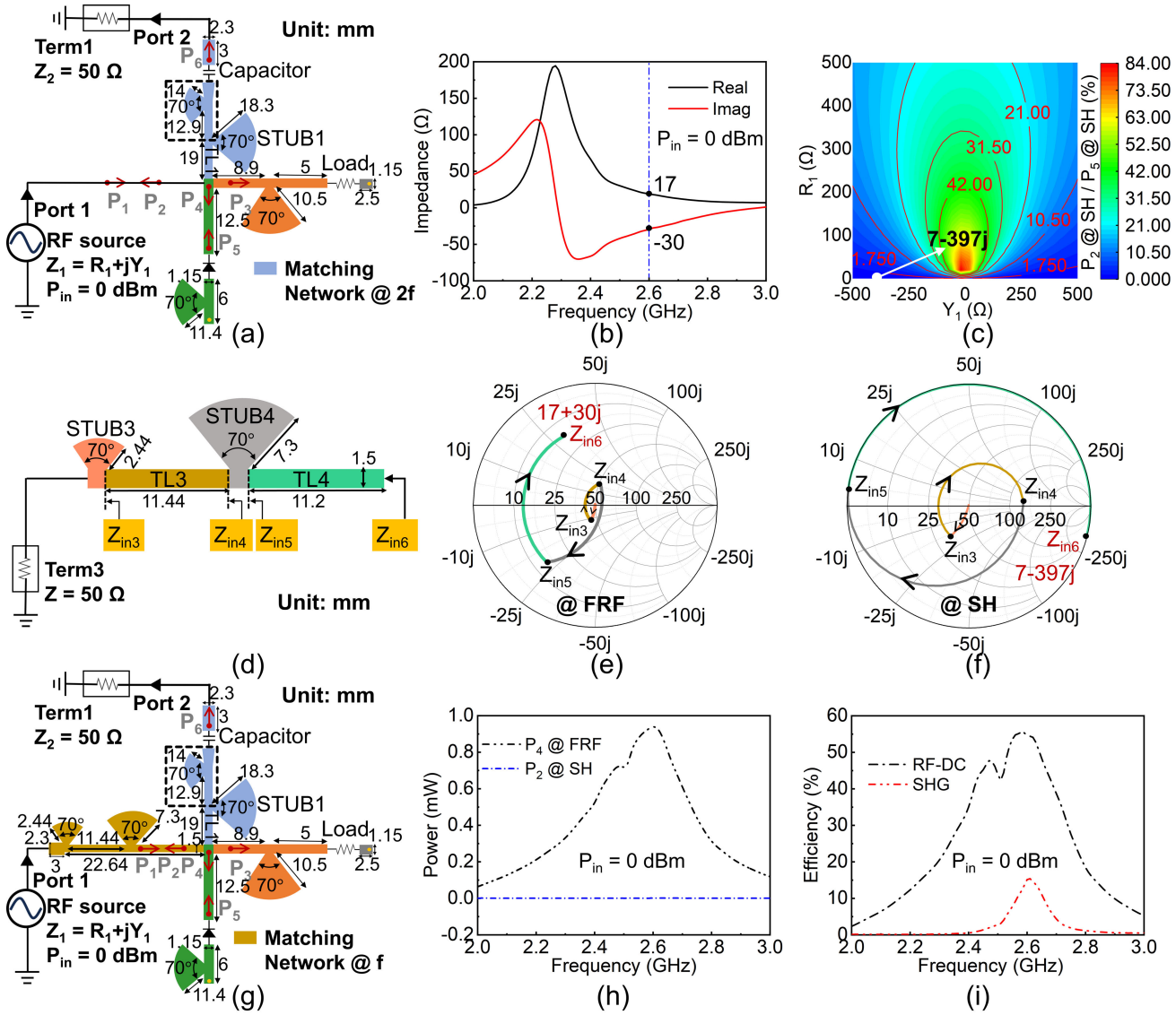

Fig. 5. (a) Structure of duplex rectifier without input matching network. (b) Simulated input impedance at Port 1. (c) Proportion of obtained SH power flowing to Port 1 versus R_1 and Y_1. (d) Design of input matching network. Trajectory changes of Z_{in3}, Z_{in4}, Z_{in5}, and Z_{in6} on the Smith chart for (e) FRF and (f) SH. (g) Structure of the proposed duplex rectifier. (h) FRF power detected by P_4 and SH power detected by P_2. (i) Simulated RF-dc efficiency and SHG efficiency of the proposed duplex rectifier.

Fig. 4(i), it is evident to find that the SH power (0.156 mW) detected by P_6 is slightly lower than that detected by P_5 (0.182 mW) due to the insert losses of microstrip structures and the capacitor. In addition, the FRF power detected by P_6 is nearly close to 0, showcasing the excellent FRF isolation feature of the output matching network. Note when to conduct the above simulations, and the input FRF power from Port 1 was always fixed to 1 mW.

3) Input Matching Network Design: Ultimately, an input matching network is needed to complete the desired duplex rectifier. Considering the ideal devices used in Fig. 2(a), the required input matching network should be equipped with the abilities of efficiently guiding the input FRF and blocking the generated SH. Regarding the first functionality, the frequency-dependent input impedance at Port 1 [see Fig. 5(a)] was initially calculated by using the ADS software, and then as shown in Fig. 5(b), the input impedance for FRF can be accurately determined as $17 - 30\text{j}\ \Omega$. Therefore, to achieve the maximum power transfer, the corresponding source impedance [namely, Z_{in6} in Fig. 5(d)] should be conjugated to the calculated input impedance. In the meantime, source pull technique was used to study the effect of the source impedance on the energy leakage ratio of the SH to the RF source, and a power probe (P_2) was placed behind Port 1 for detecting the leaked SH power to RF source. Through changing the source impedance ($R_1 + \text{j}Y_1$) of RF source, it can be observed that the energy leakage ratio (P_2 at SH/P_5 at SH) gradually decays as R_1 tends to 0 and the absolute value of Y_1 increases. Based on this conclusion, a source impedance ($7 - 397\text{j}\ \Omega$) for the SH was selected as the design target referring to the ultralow SH energy leakage ratio [white point in Fig. 5(c)].

In the following, simultaneously considering these two goals, an input matching network shown in Fig. 5(d) was designed to, respectively, transfer the standard 50-Ω impedance of Term 3 to $-17 + 30\text{j}\ \Omega$ at FRF and $7 - 397\text{j}\ \Omega$ at SH. This design consists of two radial stubs (STUB3 and

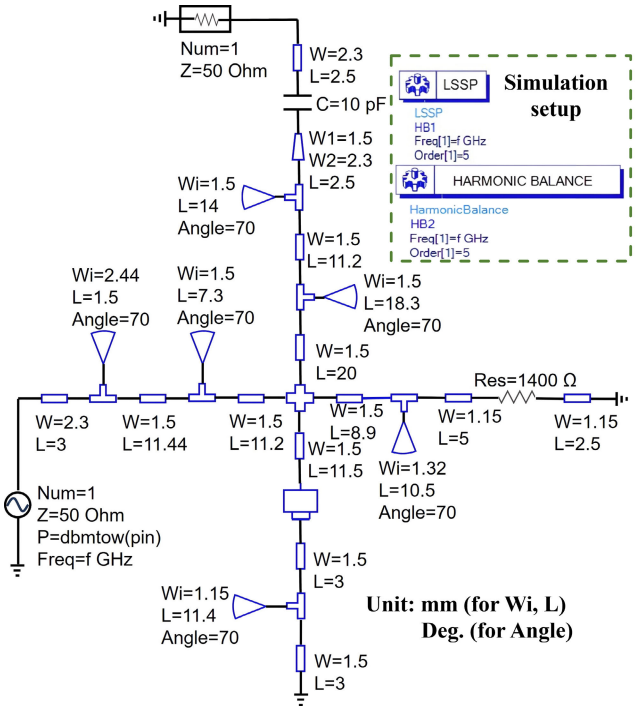

Fig. 6. ADS circuit and detailed simulation setup of the proposed rectifier.

STUB4) and two transmission lines (TL3 and TL4). With the help of STUB3, TL3, and STUB4, the initial 50-Ω impedance can be converted onto equal reflection coefficient circles of the target impedance for the FRF [Z_{in5} shown in Fig. 5(e)] and SH [Z_{in5} shown in Fig. 5(f)], respectively. Then, the endpoint of Z_{in5} [see Fig. 5(e)] can be derived from a quarter of the circle along the equal reflection coefficient circle [Z_{in6} shown in Fig. 5(e)] by introducing the TL4 with the electrical length of about one-eighth wavelength (at FRF), and finally stays on the target impedance 17 + 30j Ω [see Fig. 5(e)]. Due to the wavelength of the SH is half of the FRF's, the impedance of the SH can rotate about a half of the circle along the equal reflection coefficient circle [Z_{in6} shown in Fig. 5(f)], thus realizing the needed high imaginary part.

By now, the duplex rectifier [see Fig. 5(g)] has been completely carried out through embedding the proposed input matching network [see Fig. 5(d)] into the previously realized circuit shown in Fig. 4(h). The ADS circuit and detailed simulation setups of the proposed rectifier are provided in Fig. 6. Regarding the total system, its insertion loss was first evaluated to reflect the performance of the input matching network. As shown in Fig. 5(h), when the input FRF from Port 1 was set to 1 mW, more 0.9-mW FRF power [black dotted line in Fig. 5(h)] can successfully flow into the diode, indicating the ultralow insertion loss of the proposed input impedance matching network. In addition, the SH power detected by P_2 is mostly close to 0, conforming to the initial design requirement. Finally, the RF-dc conversion and SHG efficiency of the whole system were calculated and provided in Fig. 5(i). Compared with those in Fig. 2(d) and (e), due to the extra insertion loss induced by the microstrip structures and the capacitor, the realized RF-dc conversion (55.4%) and SHG efficiency (15.3%) slightly decay but still maintain a high level.

C. Performance Evaluation of the Duplex Rectifier

To verify our design, a prototype with the optimized structural parameters was printed on a low-cost F4B substrate with the relative permittivity of 2.2, loss tangent of 0.001, and thickness of 0.762 mm, as shown in Fig. 7(a). The reflection coefficient of the fabricated rectifier was measured with the help of a vector network analyzer (VNA, Agilent E5072A). During the measurement process, the input power from Port 1 was set to 0 dBm. In Fig. 7(b), the measured S_{11} for the FRF is below −15 dB, which is in accordance with the simulated one, indicating the good impedance matching performance of the sample. Furthermore, considering the nonlinear feature of the diode, the power-dependent S_{11} of the sample was also provided in Fig. 7(c). It is obvious that the S_{11} (for the FRF) of the proposed rectifier is always below −10 dB at an input power range of −9.5 dBm–10 dBm.

Next, to measure the RF-dc conversion and SHG efficiency of the proposed rectifier, a RF signal generator (Keysight E8257D) and analyzer (Keysight N9010A) were adopted to transmit the FRF signal with specified power level from Port 1 and receive the generated SH from Port 2, respectively, and the voltage across the load was measured by a voltmeter at the same time. The RF-dc conversion and SHG efficiency can be separately calculated by using the following equations:

$$\eta_{\text{RF-DC}} = \frac{V_{out}^2}{R \times P_{in} \text{ at } FRF} \times 100\% \tag{3}$$

$$\eta_{\text{SHG}} = \frac{P_{SH}}{P_{in} \text{ at } FRF} \times 100\% \tag{4}$$

where R is the optimal load resistance of the rectifier (1400 Ω), P_{in} at FRF denotes the input power provided by the signal generator, V_{out} presents the voltage across the load resistance, and P_{SH} denotes the detected SH power. Before calculating the RF-dc conversion efficiency of the fabricated rectifier according to (3), its output voltage versus input FRF power was first measured and shown in Fig. 7(d). As the input FRF power increases from −15 dBm to 2 dBm, the measured V_{out} gradually enhances and shows highly consistent with the simulated results. But, when input FRF power exceeds 2 dBm, the measured output voltage depicted in Fig. 7(d) continuously increases even after the diode was penetrated. This phenomenon can be attributed to the nonlinear I–V curve of the real rectifying diode. Unlike a constant straight line for simulation model, the reverse voltage increased slightly as the reverse current became infinite. Then by substituting the input FRF power and the corresponding V_{out} [see Fig. 7(d)] into (3), the RF-dc conversion efficiency was obtained and depicted in Fig. 7(f). Although the measured RF-dc conversion efficiency is slightly lower than the simulated one, they still showcase great agreement, verifying the reliability of the measurement. From Fig. 7(f), the maximum RF-dc conversion efficiency of our duplex rectifier can reach 55.2% as the input FRF power is 3 dBm. In the meantime, by substituting the measured SH power [see Fig. 7(e)] into (4), the SHG efficiency also can be calculated [see Fig. 7(f)], and a record-breaking result (10.47% at 3 dBm) has been realized with the deliberately designed rectifier.

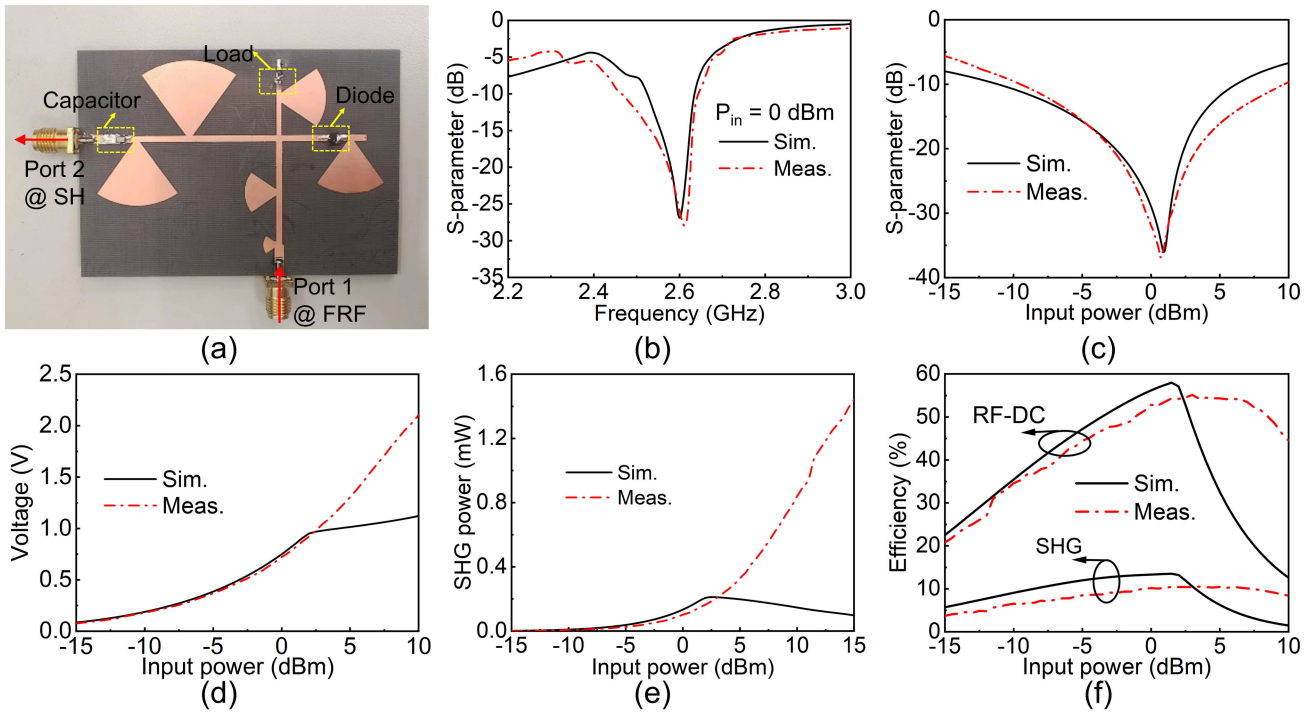

Fig. 7. (a) Photograph of the proposed rectifier. (b) Simulated and measured S_{11} of the proposed rectifier as a function of frequency with the input power level of 0 dBm. Simulated and measured (c) S_{11}, (d) dc output voltage, (e) SHG power, (f) RF-dc efficiency and SHG efficiency as a function of input power.

TABLE II
COMPARISON OF THE PROPOSED DUPLEX RECTIFIER AND RELATED DESIGNS

REF.	[21]	[22]	[23]	[24]	[30]	[31]	[32]	**This work**
FRF (GHz)	2.45	0.915	0.915	2.45	0.4645	2.4	2.6	**2.6**
Input power (dBm)	10	0	0	0	6	0	0	**0/3**
RF-DC efficiency	55%	46%	40%	54%	44.7%	59%	49.5%	**52.9%/55.2%**
Harmonic order	2	2	2	2	2	2	2	**2**
SH (GHz)	4.9	1.83	1.83	4.9	0.929	4.8	5.2	**5.2**
SHG efficiency (%)	0.06%	1.6%	1.3%	6.3%	3.15%	3.98%	1%	**10.2%/10.47%**

Finally, to exhibit the superiority of our duplex rectifier, some harmonic feedback rectenna designs have been given in Table II for comparing with ours. To the best of our knowledge, the achievement of both high-efficiency RF-dc conversion and simultaneous high SHG efficiency is a first in the field, realized by our duplex rectifier. This achievement is particularly significant as it successfully breaks through the dynamic balance typically observed between these two metrics, where higher RF-dc conversion efficiency often corresponds to lower SHG efficiency, and vice versa. Moreover, our approach represents a general strategy that, we believe, can be flexibly extended to the high-efficiency generation of higher-order harmonics. This potential is underscored by the solid results demonstrated in Fig. 7(f), suggesting a broad applicability of our method in advancing HG technologies.

III. COMMON APERTURE RX AND TX ARRAYS DESIGN

In this section, to motivate the above-obtained duplex rectifier and modulate the SH, two antenna arrays (termed as Rx array and Tx array) sharing an identical aperture will be designed to capture the incident FRF power (Rx array) and radiate the generated SH signal (Tx array), respectively.

A. Dual-Band Antenna Array Element Design

To obtain the desired Tx and Rx arrays, the realization of a dual-band antenna element is vital. Considering the octave relationship between the FRF and SH, the Rx antenna working for the FRF was first designed and illustrated in Fig. 8(a). It was constituted with a circular microstrip patch, a matching line, and a feed line with the characteristic impedance of 50 Ω.

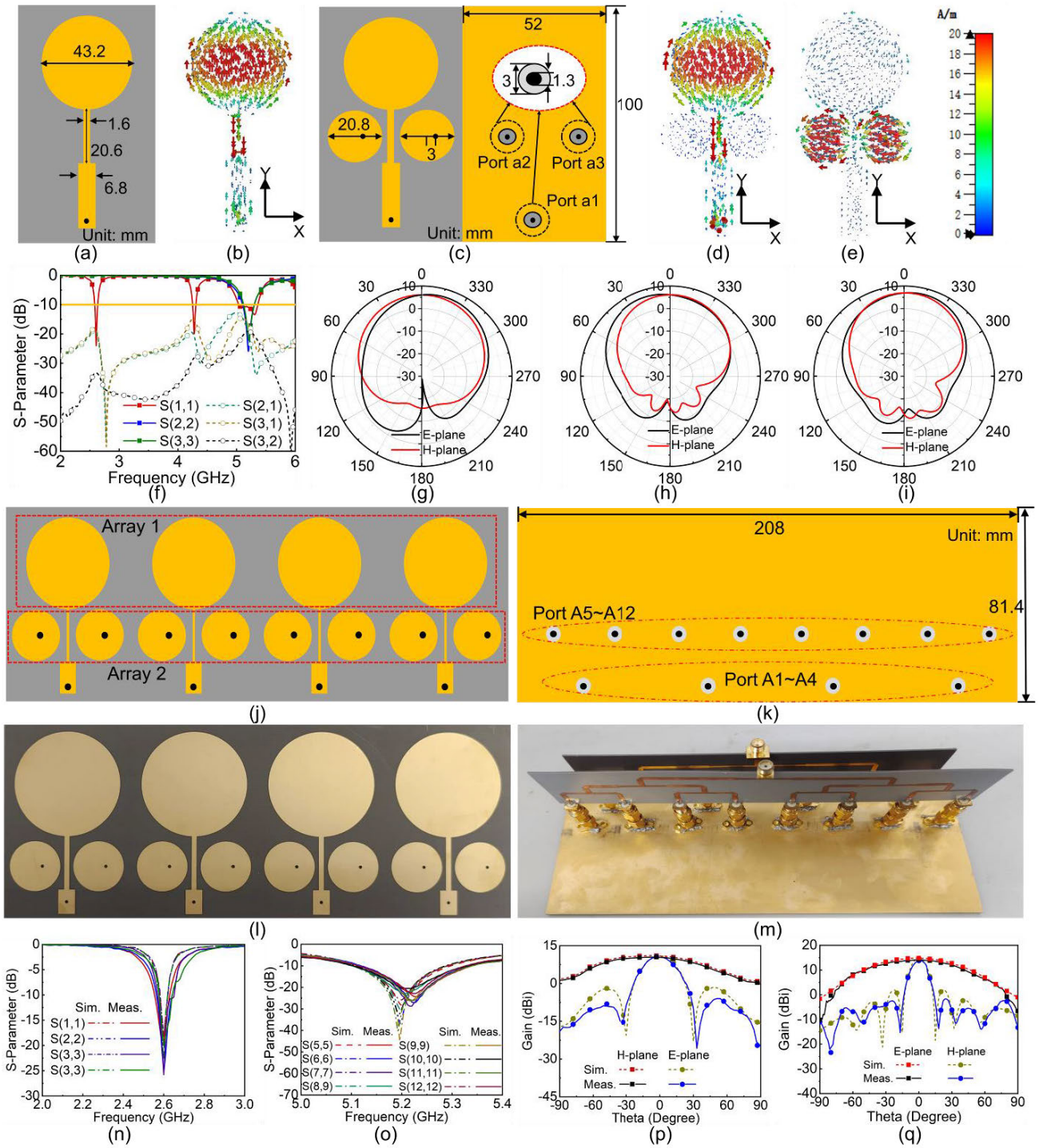

Fig. 8. (a) Structure of the Rx antenna. (b) Surface current distribution of the Rx antenna at 2.6 GHz. (c) Top and bottom views of the Rx antenna and Tx antenna. Surface current distribution of the antenna at (d) 2.6 GHz and (e) 5.2 GHz. (f) Simulated S-parameter of the Rx and Tx antenna as a function of frequency. Simulated 2-D radiation patterns of the antenna as feeding from Port a1 for (g) 2.6 GHz, (h) Port a2 for 5.2 GHz, and (i) Port a3 for 5.2 GHz. (j) Top view and (k) bottom view of the antenna array. (l) Photograph of the proposed antenna array. (m) Bottom view of antenna array connected to two power dividers. Simulated and measured (n) S-parameters for Rx antenna array and (o) Tx antenna array. Simulated and measured (p) 2-D radiation patterns of the Rx antenna array and (q) Tx antenna array.

Note that to reduce the sidelobe level of the following formed array, the lateral dimension (along x-direction) of the basic element is 52 mm smaller than the half wavelength (57.5 mm) of the FRF. In addition, this radiator was back coaxially fed [see Fig. 8(b)] to prevent the subsequently connected power divider from disturbing the radiation patterns of the Rx array. Then, the surface currents across the proposed Rx antenna were simulated to reveal the in-depth working principle. In Fig. 8(b), when fed by the FRF, the y-directional surface currents are tightly localized at the center of the circular microstrip patch, leading to the highly efficient radiation of the y-polarized wave.

Next, a couple of circular microstrip patches serving for transmitting the generated SH were positioned on the both sides of the matching line of the Rx antenna with the period of 26 mm (smaller than the half wavelength of the SH—28.75 mm) as shown in Fig. 8(c). To improve the isolation between the Rx and Tx antenna units, bias feed protype [see Fig. 8(c)] was adopted to motivate the x-directional surface currents [see Fig. 8(e)] orthogonal to that across the Rx radiator [see Fig. 8(b)]. Due to the orthogonal feature of the induced surface currents, the integration of the Rx and Tx antennas almost shows no effect with each other referring to the simulated results in Fig. 8(b), (d), and (e), resulting in the excellent port isolation performance—S_{21} (Port a1 to Port a2), S_{31} (Port a1 to Port a3), and S_{32} (Port a2 to Port a3) are all below −15 dB [see Fig. 8(f)] at the FRF and SH. Furthermore, to study the matching performance of the proposed antenna element, S_{11} (Port a1 to Port a1), S_{22} (Port a2 to Port a2), and S_{33} (Port a3 to Port a3) were also calculated with the help of the commercial software—CST Microwave Studio 2022 and provided in Fig. 8(f). The designed antenna element demonstrates effective impedance matching within the targeted frequency bands. This is a crucial aspect in ensuring optimal performance. Furthermore, to illustrate the directivity of the antenna element, simulated 2-D radiation patterns are presented when the antenna is excited from Ports a1, a2, and a3, as shown in Fig. 8(g)–(i). These radiation patterns are approximately symmetric, which is a significant attribute. This symmetry is expected to contribute to the achievement of highly directional beams that are perpendicular to the antenna aperture, especially when the elements are arranged in an array configuration. Such directional beams are essential for precise and efficient signal transmission and reception, which are key factors in advanced antenna design and application.

B. Rx and Tx Arrays Performance Evaluation

Based on the predesigned antenna element, a linear array was constructed [see Fig. 8(j) and (k)], which contains a 1 × 4 Rx array with the element spacing of 52 mm and a 1 × 8 Tx array with the element spacing of 26 mm. To evaluate its performance, a sample was fabricated on an F4B substrate with a dielectric constant of 2.2, loss tangent of 0.001 and a thickness of 2 mm, as shown in Fig. 8(l). Then, the reflection coefficients for each port of the array were simulated and measured. From Fig. 8(n) and (o), although the measured reflection coefficients have a slight difference from the simulated ones, they remain below −15 dB at FRF and −20 dB at SH, respectively, showcasing the outstanding impedance matching performance. In the following, to obtain the radiation patterns of the dual-band antenna array, two power dividers (one for the FRF, and the other for the SH) were designed to merge the feeding ports, as shown in Fig. 8(m). Then, by feeding the fabricated antenna array through the deliberately designed dividers, the E-plane and H-plane radiation patterns of the Rx [see Fig. 8(p)] and Tx arrays [see Fig. 8(q)] were measured, which agree well with the simulated ones. Due to the near-symmetric scattering patterns of the basic element shown in Fig. 8(g)–(i), the maximum gain of our array (10.78 dBi at Rx array; 14.1 dBi at Tx array) was always kept at the normal direction (Theta is equal to 0°).

IV. 8 × 8 Butler Matrix Design

To further enrich the beam behaviors of the generated SH, an 8 × 8 Butler matrix was designed to tune the propagation phase of the SH between the output matching network [blue part in Fig. 5(g)] and the Tx array. According to the topological model composed of 90° hybrid couplers, crossovers, and phase delay lines shown in Fig. 9(a), a Butler matrix [see Fig. 9(c)] was implemented, by which eight different phase gradient states were achieved at the output nodes (Port B9–B16) when fed in sequence from Port B1 to B8. Therefore, based on the array antenna theory, if the realized phase gradient states can be loaded to the Tx array, the scattering patterns of the SH will be flexibly reconstructed. Subsequently, to quantify the beam control performance, the fabricated Butler matrix [see Fig. 9(b)] was connected to the Tx array [see Fig. 9(l)] as the protype shown in Fig. 9(c), and then the corresponding 2-D scattering pattern was measured by switching the input ports. From Fig. 9(e), it is observed that as the input port is varied, the initial normal beam [as depicted in Fig. 8(q)] can be dynamically steered across an angular range of −65° to 66°. This dynamic steering capability aligns well with the simulated results presented in Fig. 9(d). Crucially, throughout the beam steering process, the gain of the transmitting (Tx) array consistently remains above 10 dBi. This observation underscores the high directivity characteristic of the array, which is a key feature for applications requiring precise directional control of the transmitted signal. The ability to maintain a high gain while steering the beam over a wide angular range illustrates the effectiveness of the antenna design in achieving both directional flexibility and signal strength.

V. Experimental Evaluation of the Total System

As of now, all components necessary for constructing a multifunctional system, which is advantageous for wireless energy harvesting, efficient SHG, and manipulation of the generated SH signal, have been assembled. The detailed working principle of the entire system is depicted in Fig. 10(a). When the frontend receiver (Rx) array captures the FRF signal, the input power is consolidated through a power divider. This consolidated power is then efficiently rectified into dc power at the backend rectifier. Simultaneously, it is converted into a SH. This dual process of power rectification and HG highlights the system's capability to not only harvest energy from ambient RF signals but also to create and manipulate SH signals, thus serving multiple functions in a single integrated system. Then, the generated SH will be led out of the circuit [orange part in Fig. 10(a)] through the predesigned output matching network and go back to the frontend Tx array along the Butler matrix. Here, for automatically controlling the beam behaviors of the generated SH, an electric RF switch (Dow-key 581-520823A) with one input port and eight output ports was added between the rectifier and Butler matrix [see Fig. 10(a)]. With the help of a microcontroller unit (MCU) (Stm32f103zet6), the "ON"/"OFF" state of each output port of the switch can be adjusted within microseconds, leading to the rapid SH beam

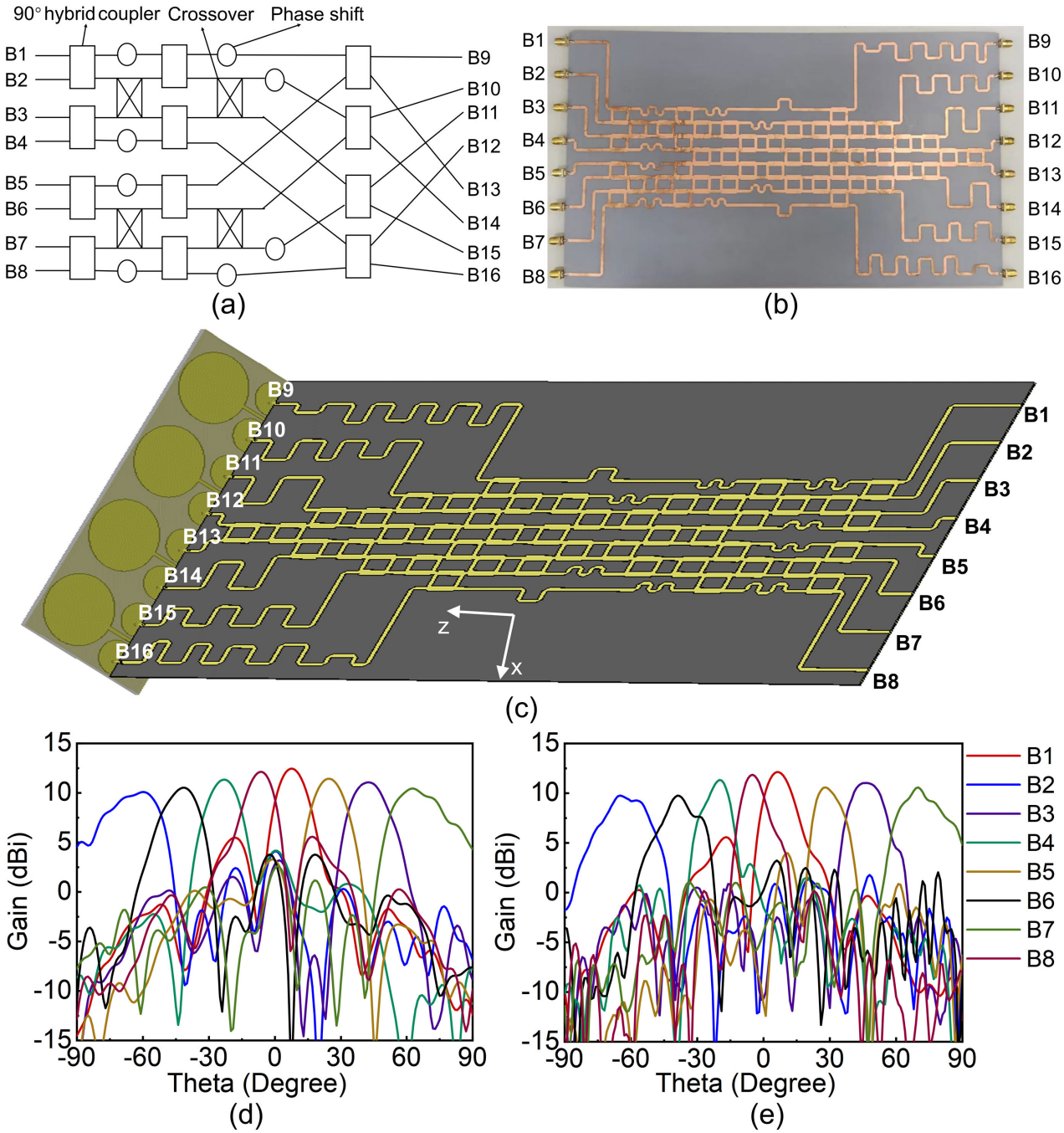

Fig. 9. (a) Structure of the conventional 8 × 8 Butler matrix. (b) Photograph of the proposed 8 × 8 Butler matrix. (c) Simulation model of antenna with Butler matrix in CST software. (d) Simulated and (e) measured radiation patterns of the proposed Tx antenna array connected to Butler matrix.

forming and scanning. The RF switch and MCU are powered by a dc source (Agilent E3620A).

According to the schematic shown in Fig. 10(a), the abovementioned multifunctional system was constructed and evaluated in a microwave anechoic chamber. When conducting the measurement, a horn antenna (LB-7180-NF) was placed at one end of a long wooden board for transmitting the FRF from a signal generator (ADF4350), and the total system was fixed to the other end. The test setup was put on a rotary system for measuring the far-field scattering patterns of the radiated SH with the help of a receiving antenna located at the far-field position. Using the test system illustrated in Fig. 10(b), the normalized radiation patterns of our system were obtained and are presented in Fig. 10(c). It is readily apparent that the measured results closely align with those depicted in Fig. 9(e). The minor fluctuations observed in the measured curves [as shown in Fig. 10(c)] can be attributed to the discontinuity characteristic inherent in the half-wave rectification mechanism, as discussed in references [33], [34]. This observation underscores the accuracy of the system's design and simulation processes, with the real-world test results largely mirroring the predicted outcomes. The identified discrepancies, explained by the characteristics of the rectification mechanism, provide valuable insights for further refinement

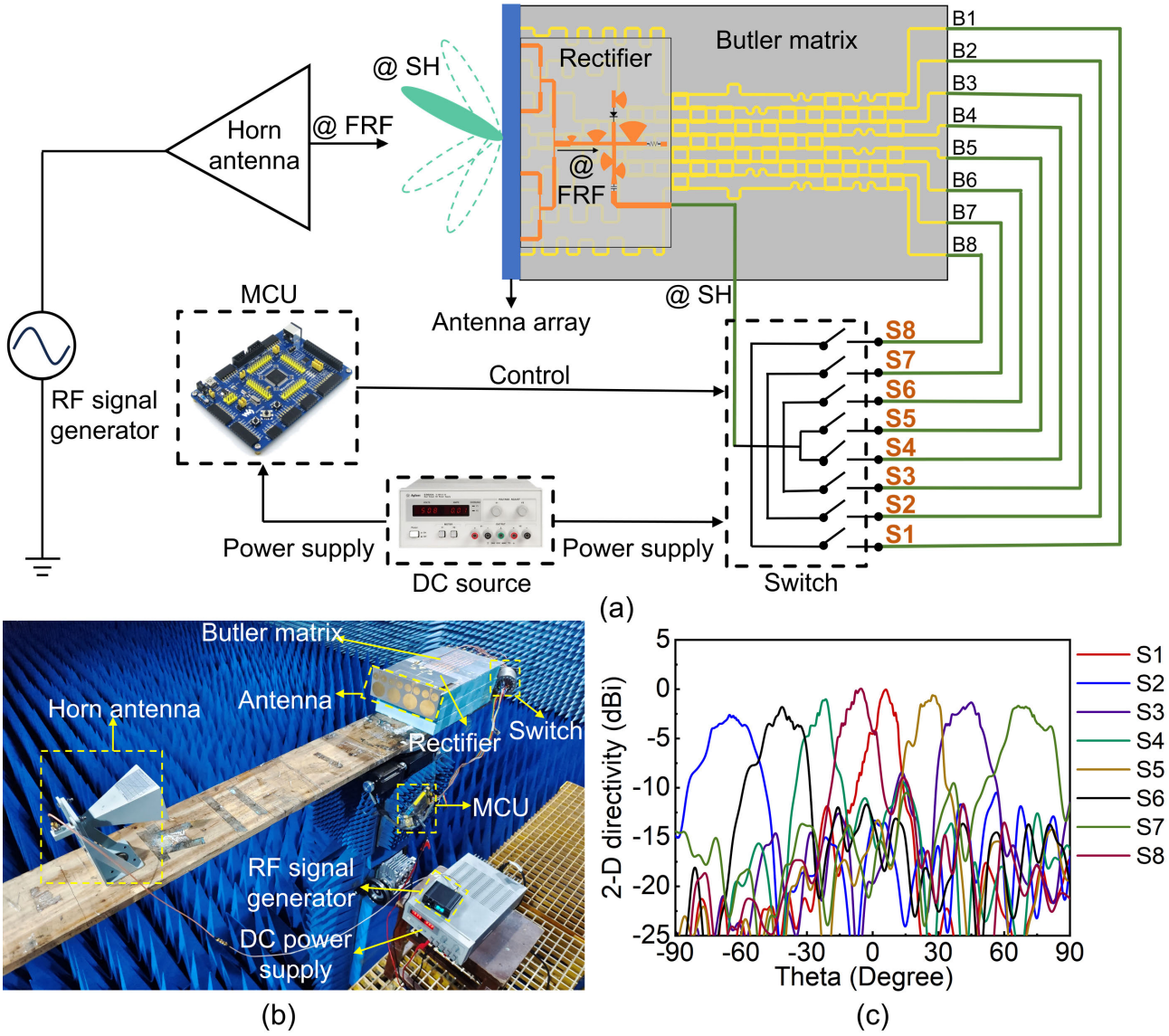

Fig. 10. (a) Working principle of the proposed multifunctional system. (b) Measurement setup in an anechoic chamber. (c) Measured normalized radiation patterns of multifunctional system.

and understanding of the system's behavior under practical conditions.

VI. Conclusion

In this work, we have theoretically demonstrated, experimentally validated, and successfully implemented a well-designed duplex rectenna paradigm capable of efficiently generating dc power (with an efficiency of 55.2% at a 3-dBm input FRF) and SH signal (with a SHG efficiency of 10.47% at a 3-dBm input FRF). Leveraging this unified platform, we achieved large-angle SH scanning performance, ranging from $-65°$ to $66°$, for the first time, facilitated by a Butler matrix and a Tx array. It is important to highlight the remarkable scalability of our system. By simply replacing the output end and load applications, a variety of enriched functionalities can be integrated. These include integrated sensing and communication (ISAC), position recognition, and backscatter communication, among others. This versatility enhances the capabilities of classical wireless energy harvesting devices, rendering our system a highly promising option for applications in the IoT, and simultaneous wireless information and power transfer (SWIPT).

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